Curriculum Vitae for Jens Sparsø

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Address

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Personal data

Born on 19th December 1955 in Silkeborg, Denmark.

Married to Ute Pørksen (M.Sc. Pharm.).
Two children: Thorsten Sparsø (born 1983) and Eske Sparsø (born 1986).

Education

1979: B.Eng. in Electrical Engineering from the Engineering Academy of Denmark.
1981: M.Sc. from the Technical University of Denmark.

Supplementary courses (list not complete)

2005-6: Completed LearningLab DTU's course programs for: (i) Assistant professor supervisors and (ii) Ph.D. supervisors.
2005-6: Completed a 4 day course on "The DTU Leadership Role"
2009: Completed a 5 ECTS course on "Pedagogical and didactic theories in university education and teaching". Danish School of Education (DPU), Aarhus University.

Employments at Technical University of Denmark (DTU)

Oct. 1981 – June 1982:	Military service.
Aug. 1982 – June 1986:	Assistant Professor, Department of Computer Science
Aug. 1986 – Dec. 2006:	Associate Professor, Department of Computer Science (From 1996: Department of Information Technology) (From 2001: Department of Informatics and Mathematical Modelling)
Jan. 2007 – Dec. 2015	Professor (Danish: Docent) (From 2012: Department of Applied Mathematics and Computer Science)
Jan. 2016 –	Full professor in Cyberphysical Systems

Employments (External and Abroad)

Sept. 1995 – June 1996:	Visiting Associate Professor of Computer Science, University of Utah, Salt Lake City, USA.
May 2002 – April 2004:	Part time consultant for SYCS, a startup developing a novel DSP-processor.

Awards

March 1991:	Radio Parts Fonden (60,000 DKR)
December 2003:	The Reinholdt W. Jorck Award (150,000 DKR)
April 2005:	Best paper award at ASYNC'06

Research

My area of research is the design of integrated circuits and digital systems including: design methods and circuit techniques, asynchronous circuits, low-power design, (application-specific) computing structures, computer organization, multi-core processors, and on-chip interconnection networks – in short hardware platforms for embedded and cyber-physical systems

My work is focused on design principles and design methods and often involves concrete applications or cases derived from actual and relevant industrial applications. I find this combination of the general perspective and the more concrete perspective fruitful and stimulating. I have always enjoyed taking active part in the work myself, and I have a keen interest in building chip and system prototypes in order to drive and evaluate my research.

Over time I have been involved in the design of a total of 12 chips that have been fabricated and tested. We are now using FPGA-boards for prototyping of synchronous as well as asynchronous circuits.

From 1999-2003 I was the head of the Thomas B. Thrige Center for Microinstruments and the Graduate School in Microelectronics. Most recently I have managed the "Network on Chip" work package in the EU FP7 funded STREP project T-CREST (2011-2014) and I am currently leading the RTEMP project that is funded by the Danish Council for Independent Research — Technology and Production Sciences (2013-2016).

I have published more than 70 papers in refereed journals and proceedings. In 2001 more than 10 years of research and teaching resulted in a textbook on asynchronous circuit design. It has become the standard textbook on the topic. In 2006 the book was translated into Chinese at the initiative of the Chinese Academy of Sciences. My work has 3100 citations (1468 since 2010) and seven of my publications are cited more than 100 times. My H-index is 21. (All figures based on data from Google Scholar, 15 December 2015).

Over time I have been advisor/co-advisor for 14 Ph.D. students (10 completed, 1 dropped and 3 underway). Two are now in academic careers, and the rest have established successful careers in research and development in national and international companies including Oticon A/S, Teklatech A/S (a startup based on results from the Ph.D.-project), ST-Ericsson (formerly Philips Research) and ARM.

Research funding

My research has been funded by several project and program grants from the Danish Technical Research Council and the Danish Council for Independent Research, by the Thomas B. Thrige foundation, by companies involved (including Oticon, GN ReSound and Nokia), by the European Commission (FP3, FP4, FP5 and FP7), and by Ph.D.-scholarships provided by the Technical University of Denmark.

Teaching

Teaching was what originally lead me in the direction of a university career. It is an activity that I enjoy very much and that I find very rewarding.

During my employment at DTU I have taught courses on digital electronics, integrated circuits, asynchronous circuits, and computer architecture and design. From 1985–95 I was the key person driving the department's

build-up of courses in integrated circuit design (including: layout, circuit design, structured design using hardware description languages, and systems architecture). In Utah I taught courses on computer architecture and low-power asynchronous circuits. After returning from Utah I have been teaching computer architecture and digital design. This shift is in line with the evolution that has taken place in the field of integrated circuit design: from layout and circuit design over synthesis-based systems-design to multi-core systems-on-chip. In the same period I have taught Ph.D. courses on asynchronous circuit design and microelectronics.

Most recently I have been the key person driving the updating of DTU's courses on Digital Electronics (02138 Digital Electronics 1, 02139 Digital Electronics 2 and 02203 Design of Digital Systems), and I am currently involved in teaching all these courses. Among the achievements is the introduction and use of FPGA technology from the first semester.

From 2005 to 2011 I was heavily involved in the development of DTU's B.Eng. study programs. I was member of a small group headed by the Dean who introduced the Conceive Design Implement Operate (CDIO) concept (www.cdio.org) as the basis for all of DTU's B.Eng. study programs. During this time I also managed the B.Eng. in IT study program. This included: accreditation, merging of teaching staff and a major revision of the study plan.

Over time I have been advisor/co-advisor for more than 70 M.Sc. and more than 10 B.Sc./B.Eng. student projects mostly in the area of digital systems design and integrated circuit design. Many projects have involved formal collaboration with companies (including: Bang and Olufsen ICE Power, Ericsson Mobile Communications, GN ReSound, LSI Logic, MAN Diesel, Merus Audio, MIPS Denmark, Nokia, Oticon, Thrane & Thrane, Vitesse Semiconductor Corporation).

I have completed LearningLab DTU's course programs for: University teachers, Assistant Professor Supervisors and PhD supervisors, as well as a 5 ECTS course on "Pedagogical and didactic theories in university education and teaching" offered by the Danish School of Education (DPU), Aarhus University. Since 2007 one of the department's Assistant Professor supervisors.

Administrative tasks

During my time at DTU I have always taken active part in the organization and administration of departmental matters, in particular in the coordination of the teaching and the development of and coordination of study programs. Some key activities are listed below.

- Member of the board of the Department of Computer Science, DTU, 1987–1995. During this time I also served periods as chairman of the studies/teaching committee and the finance/accounting committee.
- Coordinator of the M.Sc. specialization in "Computer Systems" (Danish: fagprofil i Datateknisk Konstruktion). 1993-2001. This was among the first initiatives in the department which shaped the combined hardware-software profile for which we are still known.
- Director for the Thomas B. Thrige Center for Microinstruments and the Graduate School in Microelectronics (July 1999–2003).
- From 2004 to 2008 member of a small group of faculty members supporting the head of the Computer Science and Engineering section of the department.
- From 2005 to 2011 one of 4 members of the Dean's task force who adopted and introduced the CDIO-concept (www.cdio.org) as the basis for DTU's B.Eng. study programs.
- From 2005 to 2011 Director of Studies for the B.Eng. in IT study program. Here the main challenges were:

  - Takeover of the B.Eng. study and merging of faculty form the former Engineering Academy of Denmark and from DTU.
  - Accreditation of the study program by the Danish Evaluation Institute (operating on behalf of the Danish Ministry of Education).
  - The development and implementation of a new study plan based on CDIO-principles (see: www.cdio.org and http://www.dtu.dk/Uddannelse/Diplomingenior/Introduktion-til-Diplomingenioeruddannelsen).
- From 2008 to 2009 Head of the System-on-Chip section. Rated "International level" in the 2008 research evaluation of the department. In 2009 merged into the Embedded Systems section.

Organization of scientific events

- Organizer of the "ACiD-WG workshop on Asynchronous Low-Power VLSI," Technical University of Denmark, April 11-12, 1994.
- Director and local organizer of the "Summer School on Asynchronous Circuit Design," Technical University of Denmark, August 18-22, 1997. (58 participants + 6 teachers).
- Member of the steering committee for the following conferences:
  - IEEE International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC): 1994–2002, 2006 – current.
  - Int. Workshop on Power and Timing Modelling, Optimization and Simulation (PATMOS), 1997–2001
  - ACM/IEEE International Symposium on Networks-on-Chip (NOCS), 2007 – current.
- General chair and local organizer of PATMOS'98, 8th Int. Workshop on Power and Timing Modelling, Optimization and Simulation, Technical University of Denmark, October 7-9, 1998.
- Program chair for PATMOS'99, 9th Int. Workshop on Power and Timing Modelling, Optimization and Simulation, Kos, Greece, October 7-9, 1999.
- Organizer of the Ph.D. course *Topics in Microelectronics*, DTU, fall 2001 and fall 2003.
- Program co-chair for 12th IEEE Symposium on Asynchronous Circuits and Systems, Grenoble, 2006.
- General chair and local host for 18th IEEE Symposium on Asynchronous Circuits and Systems (ASYNC 2012), and 6th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2012), May 2012 at DTU.
- Program co-chair for 21th IEEE Symposium on Asynchronous Circuits and Systems, 2015.

External talks, seminars and courses

- Half-day seminar at DTU "10 M bit/sec Viterbi decoder chip" (participants from Danish industry and academia), May 1989.
- Tutorials on design of asynchronous circuits at:
  - EURO-DAC'93, European Design Automation Conference, September 1993.
    [6 hours].

  - ESSCIRC'94, European Solid State Circuits Conference, September 1995. [4 hours]
  - Israel Workshop on Asynchronous VLSI, 19-22 March 1995.
  - ACiD-WG Winter School "Timing for Deep Sub-micron Chips", Cambridge University, 3-7 January 2005. [1 full day]

- Oticon-DTU half-day seminar on "Asynchronous circuits with low power consumption," DTU, August 15, 1997.

- A one-week intensive course (12 lectures) on asynchronous circuit design at Delft University of Technology, 3-7 May 1999.

- A one-week intensive course at STMicroelectronics, Rousset, France, 22-26 September 2003. Based on my book and DTU-course 02204 Design of Asynchronous Circuits.

- Many invited talks in Europe and USA, *including:*
  - The Society of Danish Engineers. November 1992.
  - Technical University of Munich. June 1992.
  - Department of Computer Science, Univ. of Washington, Seattle, January 1993.
  - Univ. of Linköping, NUTEK and ISY "Inbygda System rammeprogramkonferens". November 1994.
  - Department of Computer Science, Univ. of Utah, January 1996.
  - Department of Computer Science, California Institute of Technology, July 1996.
  - Electrical Engineering Department, University of Southern California, July 1996.
  - Ericsson Mobile Communications, Lund (March 1998).
  - MEL-ARI Workshop (ESPRIT IV Advanced Research Initiative in Microelectronics), Lille, France, February 1998.
  - Norchip'01, Stockholm, 12-13 November 2001. Title of talk: "Asynchronous circuit design".
  - Technical University of Lund, Sweden, "Asynchronous circuits for low power", 17 October 2001.
  - ISLPED'02, International Symposium on Low Power Electronic Design, Monterey, USA, 12-14 August 2002. Title of talk: "Future Directions in Clocking Multi-Ghz Systems".
  - SSoCC'04, Swedish Systems on Chip Conference, Båstad, Sweden, 13-14 April 2004. Title of talk: "Future Networks-on-Chip; will they be Synchronous or Asynchronous?".
  - Norchip'07, Aalborg, Denmark, 19-20 November 2007. Title of talk: "Asynchronous design of Networks-on-Chip".
  - Petri Nets 2012 and ACSD 2012, Hamburg, Germany, 28 June 2012, Keynote presentation: "Networks-on-chip for real-time multi-processor systems-on-chip".
  - The Society of Danish Engineers. 29 April 2013. Title of talk: "Networks-on-Chip for Hard Real-time Systems".

Refereeing and assessment

- January-March 2015. Academy of Finland, Research Council for Natural Sciences and Engineering. Member of review panel for research proposals in the field of Electrical Engineering.

- Referee for several journals including: IEEE Transactions on Circuits and Systems, Proceedings of the IEEE, IEEE Transactions on VLSI Systems, IEEE Transactions on CAD, Electronics letters, IEEE Design & Test of Computers, IEEE journal of Solid-State Circuits, Journal of VLSI Signal Processing, VLSI design, Integration the VLSI journal.
- Referee for several conferences including: ASYNC, DATE, ISCAS, NOCS, PATMOS, NoCArc.
- Reviewer of project proposals and ongoing projects under ESPRIT-4 (1997-2000).
- Member of assessment committees for Ph.D.-candidates (list not complete):
  - Jacques Jonsmann, Mikroelektronikcentret (MIC), DTU. Ph.D.-defense, spring 2000. Thesis title: "Technology Development for Topology Optimised Thermal Microactuators". Chairman of assessment committee.
  - Thomas Olsson, Lund University, Dept. of Electroscience. Ph.D.-defense, 3 June 2003. Thesis title: "Distributed Clocking and Clock Generation on Digital CMOS ASICs"
  - Daniel Viklund, Linköping University, Department of Electrical Engineering. Ph.D.-defense, 15 April 2005. Thesis title: "Development and Performance Evaluation of Networks on Chip".
  - Lars T. Jakobsen, Technical University of Denmark, Department of Electrical Engineering. Ph.D.-defense, 5 August 2008. Thesis title: "High performance low cost digital controlled power conversion technology". Chairman of assessment committee.
  - Omer Can Akgun, École Polytechnique Fédérale de Lausanne (EPFL), Microelectronic Systems Laboratory. Ph.D.-defense, 4 November 2009. Thesis title: "Energy Efficiency Enhancement of Sub-Threshold Digital CMOS – Modeling, Technology Selection and Architectural Exploration".
  - Ming Liu, Royal Institute of Technology (KTH), Department of Electronic Systems. Ph.D.-defense, 14 June 2011. Thesis title: "Adaptive Computing based on FPGA Run-time Reconfigurability".
  - Michael R. Boesen, Technical University of Denmark, Department of Informatics and Mathematical Modeling. Ph.D.-defense, 20 September 2011. Thesis title: "A Bio-Inspired Self-Healing Reconfigurable Hardware Architecture - Concept, design, prototype, and evaluation". Chairman of assessment committee.
  - Eslam Yahya, Grenoble Institute of Technology, December 2012. Thesis title: "Performance Modeling, Analysis and Optimization of Multi-Protocol Asynchronous Circuits".
  - Lakob Lechner, Vienna University of Technology , Ph.D.-defense 17 June 2014. Thesis title: "Building Robust GALS Circuits – Fault-Tolerant and Variation-Aware Design Techniques for Reliable Circuit Operation".
  - Laura Micconi, Technical University of Denmark, Department of Applied Mathematics and Computer Science. Ph.D.-defense, 16 December 2014. Thesis title: A Probabilistic Approach for the System-Level Design of Multi-ASIP Platforms. Chairman of assessment committee.
  - Shaoteng Liu, Royal Institute of Technology (KTH), School of Information and Communication Technology. Ph.D.-defense, 4 December 2015. Thesis title: "New circuit switching techniques for on-chip networks".
- Over the years I have been member of and chairman of several assessment committees for open positions at DTU at the levels of: external lecturer, assistant professor and associate professor.

Ph.D.-students supervised

1. J. Midtgaard. *High frequencies in digital silicon VLSI systems.* PhD thesis, Department of Information Technology, Technical University of Denmark, 1997. IT-TR:1997-5 (Principal Supervisor, Assoc. Prof. Ole Olsen).

2. Lars Skovby Nielsen. *Low-power Asynchronous VLSI Design. PhD thesis,* Department of Information Technology, Technical University of Denmark, 1997. IT-TR:1997-12.

3. Özgün Paker. *Low power digital signal processing.* PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, DTU, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2002. Report: IMM-PHD-2002-107.

4. B. G. Tomov. *Compact beamforming in medical ultrasound scanners.* PhD thesis, Technical University of Denmark, (DTU), January 2003. Report: ?? (Principal supervisor: Professor J.A. Jensen, Ørsted DTU).

5. K. F. Larsen. *Types for DSP Assembler Programs.* PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, DTU, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2004. Report: IMM-PHD-2006-162.

6. S. F. Nielsen. *Behavioral synthesis of asynchronous circuits.* PhD thesis, Technical University of Denmark, Dept. of Informatics and Mathematical Modelling, 2004. Report: IMM-PHD-2005-144.

7. Tobias Bjerregaard. *The MANGO clockless network-on-chip: Concepts and implementation.* PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, DTU, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2005. Report: IMM-PHD-2005-153.

8. Shankar Mahadevan. *Simulation-based Modeling Frameworks for Networked Multi-processor System-on-Chip.* PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, DTU, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2006. Report: IMM-PHD-2006-157.

9. Mikkel B. Stensgaard. Working title: *Asynchronous Network-on-Chip.* October 2005 - November 2007. Project not completed.

10. Matthias Bo Stuart. *Modelling, Synthesis, and Configuration of Networks-on-Chips*. PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, DTU, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2010. Report: IMM-PHD-2010-230.

11. Morten S. Rasmussen. *Support for Programming Models in Network-on-Chip-based Many-core Systems.* PhD thesis, Informatics and Mathematical Modelling, Technical University of Denmark, DTU, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2010. Report: IMM-PHD-2010-235.

12. Evangelia Kasapaki. *An Asynchronous Time-Division-Multiplexed Network-on-Chip for Real-Time Systems*. PhD thesis, Department of Applied Mathematics and Computer Science, Technical University of Denmark, Richard Petersens Plads, Building 321, DK-2800 Kgs. Lyngby, 2015. Report: DTU Compute PHD-2015; No. 361.

13. Rasmus Bo Sørensen. Working title *Hardware/Software tradeoffs in Real-Time Multiprocessor Platforms*. 2013-2016.

14. Luca Pezzarozza, Working title *Dynamic Reconfiguration in FPGA-based Multi-core Real-time Embedded Systems.* 2014-2017

List of Publications

Scientific highlights

- Our first big VLSI chip; a $R = 1/2$, $K = 7$ Viterbi decoder [j15], [c57]. A new layout topology and trace-back algorithm. Chip fully functional and tested.
- Early work on low-power design using adaptive supply voltage scaling. [c53], [j12]. Chip tested and fully functional.
- A significant asynchronous chip presented at a prestigious conference [c51] and published in a prestigious journal [j10]. Chip tested and fully functional. Power consumption was one fifth of a corresponding synchronous design used in a hearing aid manufactured by Oticon.
- A textbook on asynchronous circuit design [bk1], [ch3]. Has become the standard text and the most cited text.
- A low power multi-core ASIP chip [c49], [j9]. Chip tested and fully functional.
- Networks on chip: MANGO [c40, c39], ReNoC [c28] and Argo [c9, c12], [j1]. Argo is ongoing work that will continue.

Books

[bk1] J. Sparsø and S. Furber, editors. *Principles of asynchronous circuit design – A systems perspective*. Kluwer Academic Publishers, 2001.

Book chapters

[ch1] S. Mahadevan, F. Angiolini, R. G. Olsen, J. Sparsø, and J. Madsen. A network traffic generator model for fast network-on-chip simulation. In R. Lauwereins and J. Madsen, editors, *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*, pages 173–184. Springer, 2008.

[ch2] Shankar Mahadevan, Federico Angiolini, Jens Sparsø, Luca Benini, and Jan Madsen. A traffic injection methodology with support for system-level synchronization. In R. Reis, A. Osseiran, and H.-J. Pfleiderer, editors, *VLSI-SoC: From Systems to Silicon*, IFIP series, pages 145–161. Springer, 2007. (Extended and revised best papers from IFIP TC 10, WG 10.5, Thirteenth International Conference on Very Large Scale Integration of System on Chip (VLSI-SoC), 2005).

[ch3] J. Sparsø. Asynchronous circuit design – a tutorial. In J. Sparsø and S. Furber, editors, *Principles of asynchronous circuit design – A systems perspective*, chapter 1-8, pages 1–152. Kluwer Academic Publishers, 2001.

Journal articles

[j1] E. Kasapaki, M. Schoeberl, Rasmus Bo Sørensen, C. T. Müller, K. Goossens, and J. Sparsø. Argo: A Real-Time Network-on-Chip Architecture with an Efficient GALS Implementation. *IEEE Transactions on VLSI Systems*, 2015. (Accepted for publication).

[j2] M. Schoeberl, S. Abbaspour, B. Akesson, N. Audsley, R. Capasso, J. Garside, K. Goossens, S. Goossens, S. Hansen, R. Heckmann, S. Hepp, B. Huber, A. Jordan, E. Kasapaki, J. Knoop, Y. Li, D. Prokesch, W. Puffitsch, P. Puschner, A. Rocha, C. Silva, J. Sparsø, and A. Tocchi. T-CREST: Time-predictable Multi-Core Architecture for Embedded Systems. *Journal of Systems Architecture*. (Accepted for publication).

[j3] O. C. Akgun, J. N. Rodrigues, and J. Sparsø. Minimum energy sub-threshold self-timed circuits using current sensing completion detection. *IET Computers & Digital Techniques*, 5(4):342–353, 2011.

[j4] M. B. Stuart, M. B. Stensgaard, and J. Sparsø. The ReNoC reconfigurable network-on-chip: Architecture, configuration algorithms, and evaluation. *ACM Transactions on Embedded Computing Systems*, 10(4):45:1–45:26, 2011.

[j5] M. B. Stuart and J. Sparsø. Analytical derivation of traffic patterns in cache-coherent shared-memory systems. *Microprocessors and Microsystems (Elsevier)*, 35(7):632–642, 2011.

[j6] S. F. Nielsen, J. Sparsø, and J. Madsen. Behavioral synthesis of asynchronous circuits using syntax directed translation as backend. *IEEE Transactions on VLSI Systems*, 17(2):248–261, 2009.

[j7] Shankar Mahadevan, Federico Angiolini, Jens Sparsø, Luca Benini, and Jan Madsen. A Reactive and Cycle-True IP Emulator for MPSoC Exploration. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(1):109–122, January 2008.

[j8] T. Bjerregaard and J. Sparsø. Implementation of Guaranteed Services in the MANGO Clockless Network-on-Chip. *IEE Proceedings: Computing and Digital Techniques*, 153(4):217–229, 2006.

[j9] Ö. Paker, J. Sparsø, M. Isager, N. Haandbæk, and L. S. Nielsen. A heterogenous low-power multiprocessor architecture for audio signal processing. *Journal of VLSI Signal Processing*, 37(1):89–106, 2004.

[j10] Lars S. Nielsen and Jens Sparsø. Designing asynchronous circuits for low power: An IFIR filter bank for a digital hearing aid. *Proceedings of the IEEE*, 87(2):268–281, February 1999.

[j11] Jens Sparsø. Lavenergi kredsløb. *Naturens Verden*, (9):355–364, September 1998.

[j12] L. S. Nielsen, C. Niessen, J. Sparsø, and C. H. van Berkel. Low-power operation using self-timed circuits and adaptive scaling of the supply voltage. *IEEE Transactions on VLSI Systems*, 2(4):391–397, 1994.

[j13] Jens Sparsø and Jørgen Staunstrup. Delay-insensitive multi-ring structures. *INTEGRATION, the VLSI Journal*, 15(3):313–340, October 1993.

[j14] E. Paaske, S. Pedersen, and J. Sparsø. An area-efficient path memory structure for VLSI implementation of high speed Viterbi decoders. *INTEGRATION, the VLSI Journal*, 12(2):79–91, November 1991.

[j15] J. Sparsø, H. N. Jørgensen, E. Paaske, S. Pedersen, and T. Rübner-Petersen. An area-efficient topology for VLSI implementation of Viterbi decoders and other shuffle-exchange type structures. *IEEE Journal of Solid State Circuits*, SC-26(2):90–97, February 1991.

Conference articles

[c1] Evangelia Kasapaki and Jens Sparsø. The Argo NOC: Combining TDM and GALS. In *European conference on circuit theory and design (ECCTD)*, pages 1–4, 2015.

[c2] Rasmus Bo Sørensen, Wolfgang Puffitsch, Martin Schoeberl, and Jens Sparsø. Message Passing on a Time-predictable Multicore Processor. In *IEEE International Symposium on Real-Time Distributed Computing (ISORC)*, pages 51–59, 2015.

[c3] Martin Schoeberl, Rasmus Bo Sørensen, and Jens Sparsø. Models of Communication for Multicore Processors. In *IEEE International Symposium on Real-Time Distributed Computing (ISORC)*, pages 44–51, 2015.

[c4] Mathias Herlev, Christian Keis Poulsen, and Jens Sparsø. Open Core Protocol (OCP) Clock Domain Crossing Interfaces. In *Proc. 32th IEEE Norchip Conference*, pages ?–?, 2014.

[c5] C. T. Müller, E. Kasapaki, Rasmus Bo Sørensen, and J. Sparsø. Synthesis and Layout of an Asynchronous Network-on-Chip using Standard EDA Tools. In *Proc. 32th IEEE Norchip Conference*, pages ?–?, 2014.

[c6] I Kotleas, D.R. Humphreys, R.B. Sørensen, E. Kasapaki, F. Brandner, and J. Sparsø. A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs. In *Proc. IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, pages 151–158, 2014.

[c7] Martin Schoeberl, David VH Chong, Wolfgang Puffitsch, and Jens Sparsø. A time-predictable memory network-on-chip. In *Proceedings of the 14th International Workshop on Worst-Case Execution Time Analysis (WCET 2014)*, 2014.

[c8] Rasmus Bo Sørensen, Jens Sparsø, Mark Ruvald Pedersen, and Jaspur Højgaard. A Metaheuristic Scheduler for Time Division Multiplexed Networks-on-Chip. In *Proc. IEEE/IFIP Workshop on Software Technologies for Future Embedded and Ubiquitous Systems (SEUS)*, pages 309–316, 2014.

[c9] E. Kasapaki and J. Sparsø. Argo: A Time-Elastic Time-Division-Multiplexed NOC using Asynchronous Routers. In *Proc. IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)*, pages 45–52. IEEE Computer Society Press, 2014.

[c10] Christoph Müller, Steffen Malkowsky, Oskar Andersson, Babak Mohammadi, Jens Sparsø, and Joachim Rodrigues. A 65-nm CMOS Area Optimized De-synchronization Flow for sub-VT Designs. In *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, pages 380–385, 2013.

[c11] E. Kasapaki, J. Sparsø, R.B. Sørensen, and K.W.G. Goossens. Router Designs for an Asynchronous Time-Division-Multiplexed Network-on-Chip. In *Proc. of Euromicro Conference on Digital System Design (DSD)*, pages 319–326, September 2013.

[c12] J. Sparsø, E. Kasapaki, and M. Schoeberl. An Area-efficient Network Interface for a TDM-based Network-on-Chip. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 1044–1047, 2013.

[c13] Andreas Karlsson, Oskar Andersson, Jens Sparsø, and Joachim Neves Rodrigues. Ir-drop reduction in sub-vt circuits by de-synchronization. In *Proc. IEEE Subthreshold Microelectronics Conference*, pages 1–3, 2012.

[c14] J. Sparsø. Networks-on-chip for real-time multi-processor systems-on-chip. In *Proc. International Conference on Application of Concurrency to System Design (ACSD)*, pages 1–5, June 2012. (Keynote for Petri Nets 2012 & ACSD 2012).

[c15] Rasmus Bo Sørensen, Martin Schoeberl, and J. Sparsø. A Light-Weight Statically Scheduled Network-on-Chip. In *Proc. 30th IEEE Norchip Conference*, pages 1–6, 2012.

[c16] M. Schoeberl, F. Brandner, J. Sparsø, and E. Kasapaki. A Statically Scheduled Time-Division-Multiplexed Network-on-Chip for Real-Time Systems. In *Proc. IEEE/ACM Intl. Symposium on Networks-on-Chip (NOCS)*, pages 152–160. IEEE Computer Society Press, May 2012.

[c17] M. B. Stuart and J. Sparsø. Analytical derivation of traffic patterns in cache-coherent shared-memory systems. *Microprocessors and Microsystems (Elsevier)*, 35(7):632–642, 2011.

[c18] J. Sparsø, T. Bolander, P. Fischer, T.K. Hansen, . Høgh, M. Nyborg, C.W. Probst, and E.A. Todirica. CDIO Projects in DTUs B.Eng. in IT Study Program. In *Proceedings of the 7th International CDIO Conference*, pages 1–12. Technical University of Denmark, June 2011.

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